

WEST Search History

[Hide Items](#)
[Restore](#)
[Clear](#)
[Cancel](#)

DATE: Thursday, July 08, 2004

Hide?	<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>
	<i>DB=USPT,PGPB; PLUR=YES; OP=ADJ</i>		
<input type="checkbox"/>	L16	L15 and (retimed or retiming)	1
<input type="checkbox"/>	L15	L14 and L13	113
<input type="checkbox"/>	L14	L10 and (parsed or parsing or parse)	198
<input type="checkbox"/>	L13	L5 or ((716/17 716/18)!.CCLS.)	10348
<input type="checkbox"/>	L12	L5 and ((716/17 716/18)!.CCLS.)	420
<input type="checkbox"/>	L11	L10 and (data flow or control structure or node)	289
<input type="checkbox"/>	L10	L8	397
	<i>DB=JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>		
<input type="checkbox"/>	L9	L8	9
	<i>DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>		
<input type="checkbox"/>	L8	L7 and ((map\$ or translat\$) near3 (hardware or HDL))	406
<input type="checkbox"/>	L7	L6 and (synthesi\$ or verification)	6166
<input type="checkbox"/>	L6	hardware description or HDL	10971
	<i>DB=USPT,PGPB; PLUR=YES; OP=ADJ</i>		
<input type="checkbox"/>	L5	L4 or L3 or L2 or L1	9714
<input type="checkbox"/>	L4	((((716/2 716/3 716/4 716/5)!.CCLS.))	2823
<input type="checkbox"/>	L3	((((704/220)!.CCLS.))	314
<input type="checkbox"/>	L2	((((703/1 703/2 703/3 703/4 703/13 703/14 703/15 703/22 703/26 703/27 703/28)!.CCLS.))	4052
<input type="checkbox"/>	L1	((((717/106 717/107 717/108 717/109 717/119 717/134 717/135 717/136 717/137 717/138 717/139 717/140 717/141 717/142 717/143 717/144 717/145 717/146 717/147 717/148 717/149 717/150 717/151 717/152 717/153 717/154 717/155 717/156 717/157)!.CCLS.))	3009

END OF SEARCH HISTORY



US Patent & Trademark Office


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

Search: ☒ The ACM Digital Library ☐ The Guide

+synthesis +VHDL +Control-flow

SEARCH


THE ACM DIGITAL LIBRARY

 [Feedback](#) [Report a problem](#) [Satisfaction survey](#)

Terms used [synthesis](#) [VHDL](#) [Control flow](#)

Found 32 of 139,567

Sort results
by

 [Save results to a Binder](#)

Try an [Advanced Search](#)

Display
results

 [Search Tips](#)

Try this search in [The ACM Guide](#)

☐ Open results in a new
window

Results 1 - 20 of 32

Result page: [1](#) [2](#) [next](#)

Relevance scale ☐ ☐ ☐ ☐ ☐

1 [Java based object oriented hardware specification and synthesis](#)

Tommy Kuhn, Wolfgang Rosenstiel

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available:  [pdf\(428.53 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#)

2 [An efficient ILP-based scheduling algorithm for control-dominated VHDL descriptions](#)

Michael Münch, Norbert Wehn, Manfred Glesner

October 1997 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 2 Issue 4

Full text available:  [pdf\(375.99 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

To adopt behavioral synthesis techniques in existing design flows, the synthesis methodology must provide the designer with a mechanism to specify a component's interface timing. This will permit pre- and postsynthesis validation through cosimulation with other subsystems or even through formal verification. In control-flow dominated designs, additional timing constraints will result in a complex specification/constraint system for which the scheduling problem has been shown to be NP-complete ...

Keywords: integer linear programming (ILP), scheduling, timing constraints

3 [Behavioral network graph: unifying the domains of high-level and logic synthesis](#)

Reinaldo A. Bergamaschi

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available:  [pdf\(787.07 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

4 [An Efficient ILP-Based Scheduling Algorithm for Control-Dominated VHDL Descriptions](#)

Authors: Michael Muench, Manfred Glesner, Norbert Wehn

November 1996 **Proceedings of the 9th International Symposium on System Synthesis**

Full text available:  [pdf\(940.81 KB\)](#)

Additional Information: [full citation](#), [abstract](#)

 [Publisher Site](#)

In this paper, we present for the first time a mathematical framework for solving a special instance of the scheduling problem in control-flow dominated behavioral VHDL descriptions given that the timing of I/O signals has been completely or partially specified. It is based on a code-transformational approach which fully preserves the VHDL semantics. The scheduling problem is mapped onto an integer linear program (ILP) which can be constrained to be solvable in polynomial time, but still permits ...

Keywords: scheduling, control-flow dominated VHDL, ILP, time-constrained scheduling, resource-constrained scheduling, code transformation

5 [Analysis of different protocol description styles in VHDL for high-level synthesis](#)

M. Rahmouni, A. Jerraya, P. Kission, A. Mesquita, A. Pedroza, L. Pirmez


September 1996 **Proceedings of the conference on European design automation**

Full text available:  [pdf\(250.01 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

6 [From VHDL to efficient and first-time-right designs: a formal approach](#)

Peter F. A. Middelhoek, Sreeranga P. Rajan

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Full text available:  [pdf\(722.99 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this article we provide a practical transformational approach to the synthesis of correct synchronous digital hardware designs from high-level specifications. We do this while taking into account the complete life cycle of a design from early prototype to full custom implementation. Besides time-to-market, both flexibility with respect to target architecture and efficiency issues are addressed by the methodology. The utilization of user-selected behavior-preserving transformation steps e ...

Keywords: CDFG, SFG, VHDL, correctness by construction, design methodology, rapid system prototyping, transformational design

7 [Formulation and evaluation of scheduling techniques for control flow graphs](#)

Maher Rahmouni, Ahmed A. Jerraya


December 1995 **Proceedings of the conference on European design automation**

Full text available:  [pdf\(550.17 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

8 [FADIC: architectural synthesis applied in IC design](#)

J. Huisken, F. Welten

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available:  [pdf\(197.94 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

9 [Background memory management for dynamic data structure intensive processing systems](#)

Gjalt de Jong, Bill Lin Carl Verdonck, Sven Wuytack, Francky Catthoor

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available:

Telecommunication network management applications often require application-specific ICs that use large dynamically allocated stored data structures. Currently available hardware synthesis environments typically do not support dynamic data structure concepts and their associated memory synthesis problems. In this paper we address the \fbackground memory management\fp task in a hardware design trajectory, which includes allocation of a distributed memory architecture, assignment and mapping of a ...

Keywords: Background memory management system level design telecommunication network applications

10 [Efficient scheduling of conditional behaviors for high-level synthesis](#) 

Apostolos A. Kountouris, Christophe Wolinski

July 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 3

Full text available:  pdf(1.50 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

As hardware designs get increasingly complex and time-to-market constraints get tighter there is strong motivation for high-level synthesis (HLS). HLS must efficiently handle both dataflow-dominated and controlflow-dominated designs as well as designs of a mixed nature. In the past efficient tools for the former type have been developed but so far HLS of conditional behaviors lags behind. To bridge this gap an efficient scheduling heuristic for conditional behaviors is presented. Our heuristic a ...

Keywords: Design automation, conditional behavior, high level synthesis (HLS), scheduling

11 [An efficient multi-view design model for real-time interactive synthesis](#) 

Allen C.-H. Wu, Tedd S. Hadley, Daniel D. Gajski

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(502.62 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

12 [High level and system level synthesis: Hierarchical conditional dependency graphs as a unifying design representation in the CODESIS high-level synthesis system](#) 

Apostolos A. Kountouris, Christophe Wolinski

September 2000 **Proceedings of the 13th international symposium on System synthesis**

Full text available:  pdf(197.05 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

In high-level hardware synthesis (HLS) there is a gap on the quality of the synthesized results between data-flow and control-flow dominated behavioral descriptions. Heuristics destined for the former usually perform poorly on the latter. To close this gap, the CODESIS interactive HLS tool relies on a unifying intermediate design representation and adapted heuristics that are able to accommodate both types of designs as well as designs of a mixed data-flow and control-flow nature. Preliminary ex ...

13 [Synthesis of low-power selectively-clocked systems from high-level specification](#) 

L. Benini, P. Vuillod, G. de Micheli, Claudionor Coelho

November 1996 **Proceedings of the 9th International Symposium on System Synthesis**

Full text available:  [pdf\(1.06 MB\)](#)  Additional Information: [full citation](#), [abstract](#)
[Publisher Site](#)

In this paper we propose a technique for synthesizing low-power systems from a high-level specification. We analyze the control flow of the specification to detect mutually exclusive sections of the computation. A selectively-clocked interconnection of interacting FSMs is automatically generated and optimized where each FSM controls the execution of one section of computation. Only one of the interacting FSMs is active at any given clock cycle, while all the others are idle and their clock is st ...

Keywords: High level synthesis, low power, finite state machines, gated clocks.

14 [Hardware/software partitioning of software binaries](#)

Greg Stitt, Frank Vahid

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available:  [pdf\(290.80 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


Partitioning an embedded system application among a microprocessor and custom hardware has been shown to improve the performance, power or energy of numerous examples. The advent of single-chip microprocessor/FPGA platforms makes such partitioning even more attractive. Previous partitioning approaches have partitioned sequential program source code, such as C or C++. We introduce a new approach that partitions at the software binary level. Although source code partitioning is preferable from a p ...

Keywords: FPGA, assembly language, binary translation, codesign, decompilation, hardware/software partitioning, low power, synthesis

15 [Data and memory optimization techniques for embedded systems](#)

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg

April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2

Full text available:  [pdf\(339.91 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transformations. We next cover a broad spectrum of optimizati ...

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey

16 [Effects of resource sharing on circuit delay: an assignment algorithm for clock period optimization](#)

Subhrajit Bhattacharya, Sujit Dey, Franc Breglez

April 1998 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 3 Issue 2

Full text available:  [pdf\(260.26 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper analyzes the effect of resource sharing and assignment on the clock period of the synthesized circuit. The assignment phase assigns or binds operations of the scheduled behavioral description to a set of allocated resources. We focus on control-flow intensive descriptions, characterized by the presence of mutually exclusive paths due to the presence of nested conditional branches and loops. We show that clustering multiple operations in the same state of the schedule, p ...

Keywords: clock period, high-level synthesis, resource sharing

17 High-level techniques for signal processing: System design for DSP applications in transaction level modeling paradigm

Abhijit K. Deb, Axel Jantsch, Johnny Öberg

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available:  pdf(152.55 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


In this paper, we systematically define three **transaction level models** (TLMs), which reside at different levels of abstraction between the functional and the implementation model of a DSP system. We also show a unique language support to build the TLMs. Our results show that the abstract TLMs can be built and simulated much faster than the implementation model at the expense of a reasonable amount of simulation accuracy.

Keywords: DSP, grammar, system design, transaction level modeling

18 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2


Full text available:  pdf(385.22 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic systems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survey ...

19 Register assignment through resource classification for ASIP microcode generation

Clifford Liem, Trevor May, Pierre Paulin

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(653.28 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Application Specific Instruction-Set Processors (ASIPs) offer designers the ability for high-speed data and control processing with the added flexibility needed for late design specifications, accommodation of design errors, and product evolution. However, code generation for ASIPs is a complex problem and new techniques are needed for its success. The register assignment task can be a critical phase, since often in ASIPs, the number and functionality of available registers is limited, as t ...

20 A decade of reconfigurable computing: a visionary retrospective

R. Hartenstein

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available:  pdf(768.00 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Results 1 - 20 of 32

Result page: [1](#) [2](#) [next](#)

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2004 ACM, Inc.
[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

Useful downloads:  [Adobe Acrobat](#)  [QuickTime](#)  [Windows Media Player](#)  [Real Player](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet



Your search matched **13** of **1049776** documents.

A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or entering a new one in the text box.

☐ Check to search within this result set

Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 The concept of superprocesses for high-level synthesis and their VHDL modelling

Keresztes, P.; Agotai, I.;

Design Automation Conference, 1993, with EURO-VHDL '93. Proceedings EURO-DAC '93. European , 20-24 Sept. 1993

Pages:480 - 485

[\[Abstract\]](#)
[\[PDF Full-Text \(252 KB\)\]](#)

IEEE CNF

2 DLS: A scheduling algorithm for high-level synthesis in VHDL

O'Brien, K.; Rahmouni, M.; Jerraya, A.;

Design Automation, 1993, with the European Event in ASIC Design. Proceedings. [4th] European Conference on , 22-25 Feb. 1993

Pages:393 - 397

[\[Abstract\]](#)
[\[PDF Full-Text \(352 KB\)\]](#)

IEEE CNF

3 A data flow graph exchange standard

van Eijndhoven, J.T.J.; Stok, L.;

Design Automation, 1992. Proceedings. [3rd] European Conference on , 16-19 March 1992

Pages:193 - 199

[\[Abstract\]](#)
[\[PDF Full-Text \(568 KB\)\]](#)

IEEE CNF

4 Using global code motions to improve the quality of results for high-level synthesis

Gupta, S.; Savoiu, N.; Dutt, N.; Gupta, R.; Nicolau, A.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 23 , Issue: 2 , Feb. 2004

Pages:302 - 312

[\[Abstract\]](#) [\[PDF Full-Text \(960 KB\)\]](#) IEEE JNL

5 Functional synthesis of digital systems with TASS

Amellal, S.; Kaminska, B.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 13 , Issue: 5 , May 1994
Pages:537 - 552

[\[Abstract\]](#) [\[PDF Full-Text \(1104 KB\)\]](#) IEEE JNL

6 An efficient ILP-based scheduling algorithm for control-dominated VHDL descriptions

Munch, M.; Wehn, N.; Glesner, M.;

System Synthesis, 1996. Proceedings., 9th International Symposium on , 6-8 Nov. 1996
Pages:45 - 50

[\[Abstract\]](#) [\[PDF Full-Text \(608 KB\)\]](#) IEEE CNF

7 Analysis of different protocol description styles in VHDL for high-level synthesis

Pirmez, L.; Pedroza, A.; Rahmouni, M.; Mesquita, A.; Kission, P.; Jerraya, A.A.;

Design Automation Conference, 1996, with EURO-VHDL '96 and Exhibition, Proceedings EURO-DAC '96, European , 16-20 Sept. 1996
Pages:490 - 495

[\[Abstract\]](#) [\[PDF Full-Text \(616 KB\)\]](#) IEEE CNF

8 Formulation and evaluation of scheduling techniques for control flow graphs

Rahmouni, M.; Jerraya, A.A.;

Design Automation Conference, 1995, with EURO-VHDL, Proceedings EURO-DAC '95., European , 18-22 Sept. 1995
Pages:386 - 391

[\[Abstract\]](#) [\[PDF Full-Text \(448 KB\)\]](#) IEEE CNF

9 Semi-dynamic scheduling of synchronization-mechanisms

Ecker, W.;

Design Automation Conference, 1995, with EURO-VHDL, Proceedings EURO-DAC '95., European , 18-22 Sept. 1995
Pages:374 - 379

[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) IEEE CNF

10 From behavioral description to systolic array based architectures

Balboni, A.; Costi, C.; Fummi, F.; Sciuto, D.;

European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings. , 28 Feb.-3 March 1994
Pages:657

[\[Abstract\]](#) [\[PDF Full-Text \(92 KB\)\]](#) IEEE CNF

11 Optimized concurrent interleaving architecture for high-throughput turbo-decoding

Thul, M.J.; Gilbert, F.; Wehn, N.;

Electronics, Circuits and Systems, 2002. 9th International Conference on , Volume: 3 , 15-18 Sept. 2002

Pages:1099 - 1102 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) IEEE CNF

12 Hardware synthesis of an ATM multiplexer from SDL to VHDL: a case study

Horn, W.; Svantesson, B.; Kumar, S.; Jantsch, A.; Hemani, A.;

VLSI '99. Proceedings IEEE Computer Society Workshop On , 8-9 April 1999

Pages:100 - 105

[\[Abstract\]](#) [\[PDF Full-Text \(52 KB\)\]](#) IEEE CNF

13 Scheduling of a control data flow graph

Amellal, S.; Kaminska, B.;

Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on , 3-6 May 1993

Pages:1666 - 1669 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(408 KB\)\]](#) IEEE CNF

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved

Searching for **vhdl and synthesis and flowgraph**.

Restrict to: [Header](#) [Title](#) Order by: [Expected citations](#) [Hubs](#) [Usage](#) [Date](#) Try: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [CSB](#) [DBLP](#)

5 documents found. Order: number of citations.

[Debugging of Behavioral VHDL Specifications by Source.. - Koch, Kebschull.. \(1995\)](#) [\(Correct\)](#) [\(4 citations\)](#)

Debugging of Behavioral **VHDL** Specifications by Source Level Emulation Gernot since hw/sw codesign usually implies high level **synthesis** for the hardware parts. Thus, the RT which the **VHDL** specification is translated. This **flowgraph** mainly contains operations like www.fzi.de/sim/publications/1995002-paper.pdf

[System Validation by Source Level Emulation of.. - Koch, Kebschull..](#) [\(Correct\)](#)

Validation by Source Level Emulation of Behavioral **VHDL** Specifications Gernot Koch 1 Udo Kebschull since hw/sw codesign usually implies high level **synthesis** for the hardware parts. Thus, the RT which the **VHDL** specification is translated. This **flowgraph** mainly contains operations like www.fzi.de/sim/publications/1995003-paper.pdf

[A Transformation for Integrating VHDL Behavioral Specificatio:n - With Synthesis And](#) [\(Correct\)](#)

A Transformation for Integrating **VHDL** Behavioral Specificatio:n with **Synthesis** and Integrating **VHDL** Behavioral Specificatio:n with **Synthesis** and Software Generation Frank Vahid, Sanjiv wait statement are explained with the help of the **flowgraph** of Figure 3(a)The function current_time www.cs.ucr.edu/~vahid/pubs/eurodac94_transf.pdf

[VHDL Synthesis System \(VSS\) User's Manual Version 5.0 - Loganath Ramachandran Viraphol \(1992\)](#) [\(Correct\)](#)

. **VHDL Synthesis System (VSS) User's Manual Version 5.0** www.ics.uci.edu/pub/cad/cadlab-trs/1992/TR-92-52.VSS5.0_userman.ps.gz

[Synthesizing Hardware for Neural Networks with CADDY/CALLAS - Speckmann, Thole, Rosenstiel](#) [\(Correct\)](#)

have to be written by the designer using **VHDL**. This description can be automatically mapped onto **Synthesizing Hardware for Neural Networks with synthesis** are flow graphs generated by a **flowgraph** compiler from a **VHDL** behavioural description of www-ti.informatik.uni-tuebingen.de/~speckman/.papers/krakau.ps

Try your query at: [Google \(CiteSeer\)](#) [Google \(Web\)](#) [CSB](#) [DBLP](#)

CiteSeer - Copyright [NEC](#) and [IST](#)